FPGA Implementation of Simulated Kalman Filter Algorithm



FPGA Implementation Of Simulated Kalman Filter Optimization Algorithm

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Introduction

- 1. As the nonlinear problems of various fields are more and more complex, optimisation becomes one of the most important topics in many disciplines.
- 2. Optimisation algorithm mainly acts to obtain the best result from a solution set by given situation. Conventional optimisation algorithms perform intolerably complex calculation when meeting the nonlinear optimisation.
- 3. As the development of the electronics and information industry, the real-time requirement for high processing speed becomes more and more sincere. Thus, this project presents a novel hardware implementing method for speeding up the SKF processing speed.



Problem Statement

- 1. The processing speed of SKF on software soley can no longer meet the real-time requirements, such as positioning system and signal processing.
- 2. As an example, high processing speed is requirement in positioning the objects that is moving fast. The software is to slow to capture the current right position after every few times of iteration.
- 3. Besides, independent platform is always desired instead of relying on the software for all time.
- 4. Therefore, novel hardware implementing method is proposed for speeding up the SKF processing speed.



Objectives

- 1. To implement Simulated Kalman Filter optimisation algorithm using Verilog / VHDL.
- 2. To implement and evaluate the performance of the algorithm on FPGA.
- 3. To implement the proposed structure on FPGA (Xilinx).
- 4. To evaluate the performance of the structure in terms of speed, cost and its accuracy on Spartan-3E.



Methodology





Convergence Rate



Hardware Implementation of SKF Slowest Convergence Speed



Reliability Test

	Hardware SKF	Hardware PSO	Software SKF
Accuracy	~	✓	✓
Reliability	65%	95%	75%
Discrepancy	0.10%	0.01%	

Hardware SKF	Hardware SKF	Hardware PSO	Software SKF
Average			
convergence			
speed	296.7385ns	1047.5789ns	7644.8300us



Chip Utilization

			Chip	
	Development		Cost(logic	Chip Cost
Types	Tool	FPGA Model	block)	(IO block)
SKF	Xilinx ISE 14.7	3s500efg320-5	5864	20
PSO	Xilinx ISE 14.7	3s500efg320-5	8097	20



Power consumption

	SKF	PSO	
On-Chip	Power (mW)	Power (mW)	
Clocks	0.01	0.01	
Logic	4.7	0.24	
Signals	2.81	0.31	
IOs	0.13	0.13	
BRAMs	0	0	
MULTs	0	0	
Static Power	82.7	82.61	
Total	90.34	83.3	



Conclusion

- 1. Optimisation algorithms attract more and more worldwide attention while SKF algorithm is a novel solution for the complex nonlinear optimization.
- 2. Through this project, it has proven that the hardware implemented Simulated Kalman Filter (SKF) is suitable to be used in solving complex nonlinear various. This system is fast and it fulfils the real-time requirement for high processing speed in the electronics and information industry.
- 3. Besides, the performances of hardware implemented SKF, hardware implemented PSO and software implemented SKF are compared.

