



Chapter 5: Project Planning and Designing Tools



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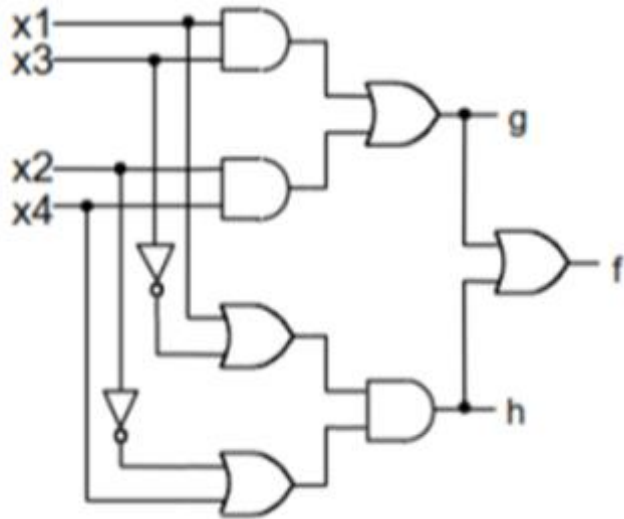
FPGA Generic Design Flow

- Design Entry
 - Create design :- Schematic or HDL
- Design Implementation
 - Partition
 - Place
 - Route

} create bit stream file
- Design Verification
 - Use simulator to check functionality
 - Check operation after loading

FPGA Generic Design Flow

- Design Entry
 - Create design :- Schematic or HDL



// Example 4

```
module example4 (x1, x2, x3, x4, f, g, h);  
  input x1, x2, x3, x4;  
  output f, g, h;
```

```
  assign g = (x1 & x3) | (x2 & x4);  
  assign h = (x1 | ~x3) & (~x2 | x4);  
  assign f = g | h;
```

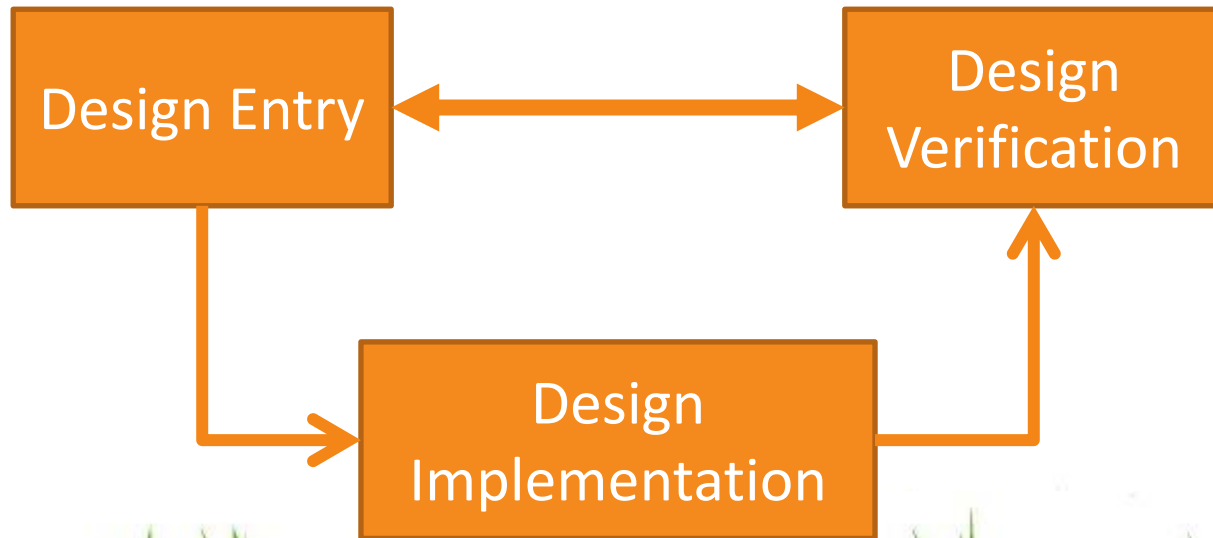
```
endmodule
```

FPGA Generic Design Flow

- Design Implementation
 - Implementing HDL to FPGA (something that fpga can use)
 1. Partition
 2. Place
 3. Route

FPGA Generic Design Flow

- Design Verification
 - Use simulator to check functionality
 - Check operation after loading



Verification Plan

Types of verification

- Simulation
 - simulate the HDL code with no timing information
 - simulate the synthesized with no timing information
- Static timing analysis (STA)
 - Compares the implemented design to specified timing constraints

Verification Plan

- Bench Testing
 - Test a physical system (prototype) in a controlled environment (lab)
- Field testing
 - Test the final product in a real-world environment



FPGA Generic Design Flow

- Combinational Logic must be covered by 4-input and 1-output “gate” – done in translation process.
- FF from the circuit must map to FPGA FF.
- Placement in general attempts at wiring minimization.
 - Wiring increases → delay increase → speed decreases

Introduction to Xilinx ISE

- Tool to configure FPGA provided by Xilinx
- Integrated Software Environment
 - Integrated collection of tools with GUI (user friendly). Eg: XST, PACE, CoreGen, Constraint Editor, Impact
- Support all the steps required to complete the design

Xilinx development flow


1. Design Entry

- .sch, .v , .vhd

2. Synthesis : use XST (Xilinx Synthesis Tool)

- Produces a netlist file starting from an HDL/Schematic description
- Converts .sch, .v , .vhd → .ngc (netlist file)

3. Translate : NGD Build

- Reads all input design netlists and then write the results in a single merged file, that describes logic circuit constrains.
- 

Xilinx development flow

3. Translate : NGD Build

- NGD is Native Generic Database: describes the logic design reduced to xilinx primitives

4. Mapping

- Maps the logic on device components
- Takes the netlist and group the logical element into CLB and IOBs
- Generate NCD and PCF
- NCD (Native Circuit Description)
 - Represents the physical circuit description of the input design as applied to a specific device → device dependent

Xilinx development flow

5. Place and Route

- Determines the placement of the cells and the routing between the cells
- PCF (Physical Constrains File)
 - Contains physical constrains
 - Info about which CLB can be used and which CLB cannot be used (increase delay)

6. Bit Stream Generation

- A bit stream is a stream of data that contains the location information for logic on a device

7. Configuration/Programming

- Download a bit file into FPGA using JTAG port
- 



HDL compiler → XST

Simulator → Xilinx ISEsim

Core Generator & Arch. Wizard → CoreGen

Pinout and Area Constrain Editor → PACE

Implementation → Translate/MAP/P&R

Device Configuration → IMPACT



Project Navigator

The screenshot displays the ISE Project Navigator interface for a project named 'uart_led'. The interface is divided into several panels:

- Design Overview:** A tree view on the left showing the project hierarchy, including 'uart_led' and its sub-components like 'xc6slx45t-3fgg484' and 'meta_harden_rst_i0 - meta_har...'. An orange callout box labeled 'Sources in project' points to this area.
- Project Status:** A table showing project details such as 'Project File: uart_led.xise', 'Module Name: uart_led', 'Target Device: xc6slx45t-3fgg484', and 'Implementation State: Synthesized'. An orange callout box labeled 'Work Area' points to this section, with a note stating 'Can show RTL Schematics, text editor or design summary'. A line from this callout points to the 'Design Summary (Synthesized)' window at the bottom.
- Device Utilization Summary:** A table showing logic utilization for various components. An orange callout box labeled 'Work Area' also points to this table.
- Detailed Reports:** A table listing reports such as 'Synthesis Report' with their status and generation dates.
- Warnings:** A console at the bottom showing warning messages from the HDLCompiler and Xst. An orange callout box labeled 'Message console' points to this area.
- Processes:** A panel on the left showing the status of various processes, with an orange callout box labeled 'Processes for source' pointing to it.

Property	Value	Property	Value
Project File:	uart_led.xise	Parser Errors:	No Errors
Module Name:	uart_led	Implementation State:	Synthesized
Target Device:	xc6slx45t-3fgg484		
Product Version:	ISE 13.4		
Design Goal:	Balanced		
Design Strategy:	Yilinx Default (unlocked)		
Environment:	System Settings		

Logic Utilization	Used	Percentage
Number of Slice Registers	0	0%
Number of Slice LUTs	42	0%
Number of fully used LUT-FF pairs	32	57%
Number of bonded IOBs	12	4%
Number of BUFG/BUFGCTRLs	1	6%

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Mon 3, Mar 10:52:48 2014	0	3 Warnings (3 new)	2 Infos (2 new)

```
WARNING:HDLCompiler:413 - "E:\Courses\BEE4563 Rapid Digital System Prototyping\Lab\training\ISE_DF\labs\intro_lab\spartan6\verilog\uart_baud_gen.v" Line 110: Result c
WARNING:HDLCompiler:413 - "E:\Courses\BEE4563 Rapid Digital System Prototyping\Lab\training\ISE_DF\labs\intro_lab\spartan6\verilog\uart_baud_gen.v" Line 122: Result c
WARNING:Xst:2677 - Node <uart_rx_i0/uart_rx_ctl_i0/frm_err> of sequential t
```

Foundation Series ISE Software

- ❑ ISE® Design Suite
 - ❑ Integrated Synthesis Environment
 - ❑ Project Navigator
 - ❑ ChipScope™ Pro Tool
 - ❑ Embedded Development Kit
- ❑ WebPACK™ software

Xilinx Design Process

- Step 1: Design Entry
 - HDL (Verilog or VHDL)
- Step 2: Synthesis
 - Translate HDL files into a netlist
- Step 3: Implementation
 - Translate, Map, Place & Route
- Step 4: Configuration
- Simulation can occur after Steps 1, 2, or 3

Xilinx Design Process

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Tool and Processes

Design entry

Synthesis

Implementation

Configuration

Additional Tool

The screenshot shows the ISE Project Navigator interface. The main window displays the 'Design Summary/Reports' tree for a project named 'uart_led'. The tree is organized into several categories, with orange arrows pointing from text labels on the left to these categories:

- Design entry:** Points to the 'Design Utilities' and 'User Constraints' sections.
- Synthesis:** Points to the 'Synthesize - XST' section, which includes 'View RTL Schematic', 'View Technology Schematic', 'Check Syntax', and 'Generate Post-Synthesis Simulation Model'.
- Implementation:** Points to the 'Implement Design' section, which includes 'Translate', 'Map', and 'Place & Route'.
- Configuration:** Points to the 'Generate Programming File', 'Configure Target Device', and 'Generate Target PROM/ACE File' sections.
- Additional Tool:** Points to the 'Manage Configuration Project (iMPACT)' and 'Analyze Design Using ChipScope' sections.

The right-hand pane shows the 'Design Overview' and 'Errors and Warnings' sections. The 'Design Overview' includes a 'Summary' section with various reports like 'IOB Properties', 'Module Level', 'Timing Constraints', 'Pinout Report', 'Clock Report', and 'Static Timing'. The 'Errors and Warnings' section lists 'Parser Messages', 'Synthesis Messages', 'Translation Messages', 'Map Messages', 'Place and Route Messages', 'Timing Messages', and 'Bitgen Messages'. The 'Detailed Reports' section includes 'Synthesis Report', 'Translation Report', and 'Map Report'. The 'Design Properties' section has checkboxes for 'Enable Message Filter', 'Optional Design Summary', 'Show Clock Reports', 'Show Failing Constraints', 'Show Warnings', and 'Show Errors'.

The bottom pane shows the 'Warnings' section with three warning messages:

- WARNING: HDLCompiler: 413 - "E:\Courses\BEE4563 Rapid Digital System Prototyping\Lab\training\IS"
- WARNING: HDLCompiler: 413 - "E:\Courses\BEE4563 Rapid Digital System Prototyping\Lab\training\IS"
- WARNING: Xst: 2677 - Node <uart_rx_i0/uart_rx_ctl_i0/frn_err> of sequ