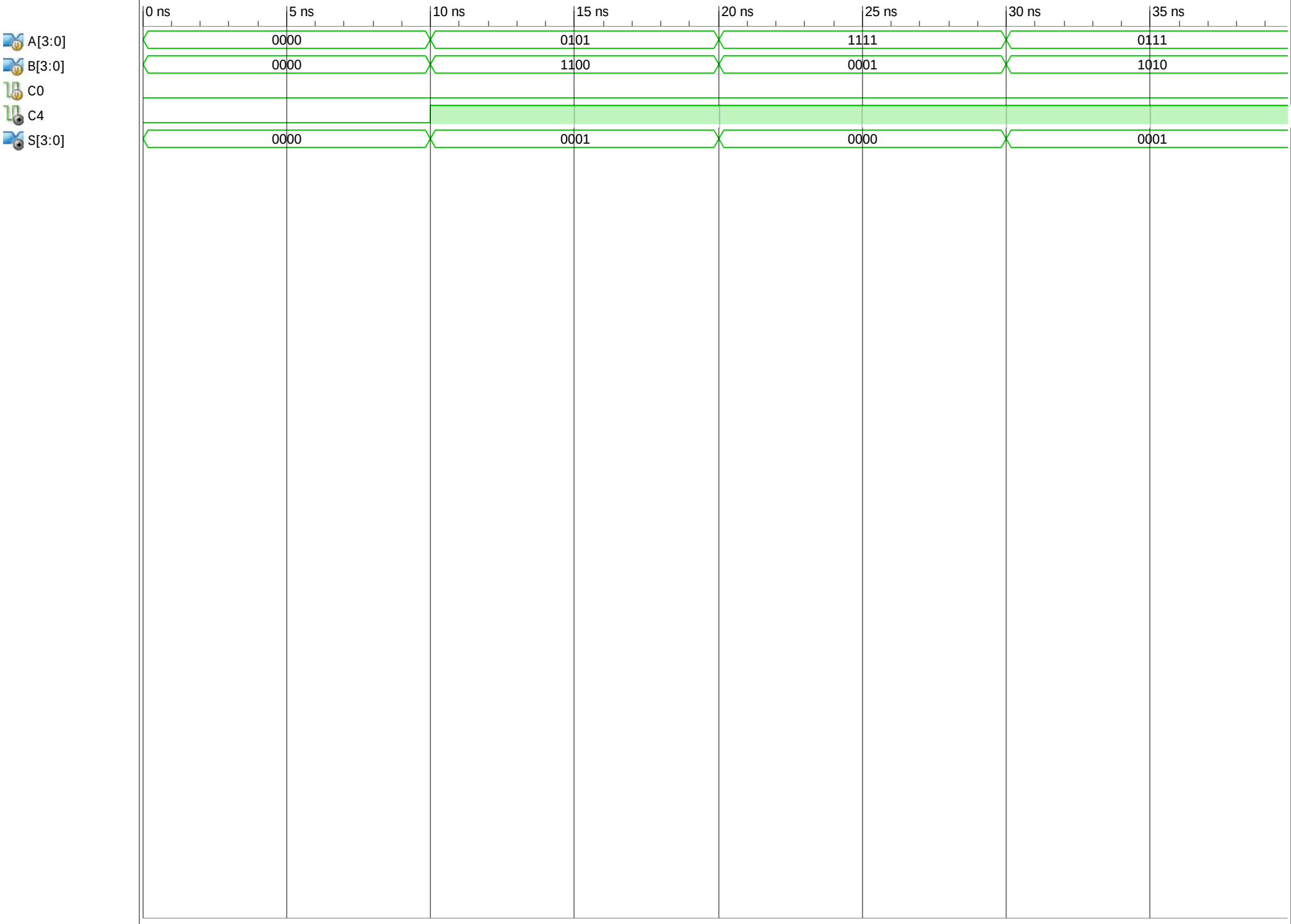
```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Company:
4   // Engineer: RMT
5   //
6   // Create Date:    15:55:55 04/25/2016
7   // Design Name:
8   // Module Name:    fa1
9   // Project Name:
10  // Target Devices:
11  // Tool versions:
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21  module fa1(
22      input A,
23      input B,
24      input Cin,
25      output Cout,
26      output S
27      );
28
29      assign S=A^B^Cin;
30      assign Cout=(A^B)&Cin|(A&B);
31
32
33  endmodule
34
```

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Company:
4   // Engineer:
5   //
6   // Create Date:    16:05:52 04/25/2016
7   // Design Name:
8   // Module Name:    fa4
9   // Project Name:
10  // Target Devices:
11  // Tool versions:
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21  module fa4(
22      input [3:0] A,
23      input [3:0] B,
24      input C0,
25      output [3:0] S,
26      output C4
27      );
28      wire [3:1] C;
29
30      fa1 add0(A[0],B[0],C0,C[1],S[0]);
31      fa1 add1(A[1],B[1],C[1],C[2],S[1]);
32      fa1 add2(A[2],B[2],C[2],C[3],S[2]);
33      fa1 add3(A[3],B[3],C[3],C4,S[3]);
34
35
36  endmodule
37
```

```
1   `timescale 1ns / 1ps
2
3   //////////////////////////////////////////////////////////////////////////////////
4   // Company:
5   // Engineer:
6   //
7   // Create Date:   16:16:01 04/25/2016
8   // Design Name:   fa4
9   // Module Name:   C:/Users/rajamohd/Documents/project
    xilinx/full_adder210416/test_fa4.v
10  // Project Name:  full_adder210416
11  // Target Device:
12  // Tool versions:
13  // Description:
14  //
15  // Verilog Test Fixture created by ISE for module: fa4
16  //
17  // Dependencies:
18  //
19  // Revision:
20  // Revision 0.01 - File Created
21  // Additional Comments:
22  //
23  //////////////////////////////////////////////////////////////////////////////////
24
25  module test_fa4;
26
27     // Inputs
28     reg [3:0] A;
29     reg [3:0] B;
30     reg C0;
31
32     // Outputs
33     wire [3:0] S;
34     wire C4;
35
36     // Instantiate the Unit Under Test (UUT)
37     fa4 uut (
38        .A(A),
39        .B(B),
40        .C0(C0),
41        .S(S),
42        .C4(C4)
43     );
44
45     initial begin
46        // Initialize Inputs
47        A = 0;
48        B = 0;
49        C0 = 0;
50
51        // Wait 100 ns for global reset to finish
52        #10;
53
54        // Add stimulus here
55        A = 4'b0101; B = 4'b1100; C0 = 0; // Using 4-bit numbers in binary format (5+12)
56        # 10 A = 4'hF; B = 4'h1; C0 = 0; // Using 4-bit numbers in hexadecimal format
```

```
      (15+1)
  57          # 10 A = 7; B = 10; C0 = 0; // Using numbers in decimal format (7+10)
  58          # 10 $finish;
  59
  60        end
  61
  62    endmodule
  63
  64
```


0 ns
5 ns
10 ns
15 ns
20 ns
25 ns
30 ns
35 ns
A[3:0]
0000
0101
1111
0111
B[3:0]
0000
1100
0001
1010
C0
C4
S[3:0]
0000
0001
0000
0001