Course Name : Electronic System Design
Course Code : BEE3233
Pre Requisite : BEE1213
Course Type : Core Program
Program Offered : BEE

Credit Hour : 3
Lecture Hours : 3
Tutorial Hours : -
Lab Hours : 2

Synopsis

In this course, digital design is taught at a higher level of abstraction than BEE1213. It provides an in-depth coverage of systematical development and synthesis of digital system with emphasis on Field Programmable Gate Array (FPGA) technology. It covers with the proper planning techniques, design strategy and tools, functional verification and system implementation. The information gained can be applied to any digital design by using a top-down synthesis design approach. Through this course, student will be able to create digital design faster, shorten development time and lower the development costs.

Course Outcomes

At the end of this course student should be able to:

CO 01: Apply knowledge of digital electronic to realize the combinational logic system, arithmetic circuit and finite state machine using different technologies.

CO 02: Design digital electronic system using combinational logic, arithmetic circuit and finite state machine (FSM) for various applications.

CO 03: Construct digital electronic system using Hardware Description Language (HDL) and implement the system on FPGA.

CO 04: Apply ethical principles and commit to responsibilities and norms of engineering practice in learning activities.

CO/PO Mapping

	PO 01	PO 02	PO 03	PO 04	PO 05	PO 06	PO 07	PO 08	PO 09	PO 10	PO 11	PO 12
CO 01	20											
CO 02			30									
CO 03			30									
CO 04								20				

Syllabus

1.0 Introduction to Digital Electronics Systems (6 Hours)

1.1 Introduction to Digital Electronic Systems
1.2 Introduction to PLD, PLA, PAL.
1.3 FPGA Technologies
1.4 FPGA versus ASIC

(BT Level 2: Understanding)

2.0 Arithmetic Logic Unit (6 Hours)

2.1 Adder
2.2 Multiplier
2.3 Arithmetic Logic Unit (ALU)

(BT Level 3: Applying)

3.0 Finite State Machines (6 Hours)

3.1 Review on counter design.
3.2 State Diagrams for FSM
3.3 Moore & Mealy Models.
3.4 Design of Sequence Detectors.

(BT Level 3: Applying)

4.0 Multiple Input Multiple Output FSM (6 Hours)

4.1 Design of Up/Down Counter without and with Enable.
4.2 Design of Vending Machine.

(BT Level 3: Applying)

5.0 Project Planning and Designing Tools (3 Hours)

5.1 Project Planning
5.2 Projects in the Project Navigator
5.3 HDL Synthesis and XST
5.4 Constraints and the I/O Planner
5.5 ISim Simulator

(BT Level 6: Creating)

6.0 Introduction to HDL (6 Hours)

6.1 Project Planning
6.2 Hardware Modelling Overview
6.3 HDL Language Concepts
6.4 Modules and Ports
6.5 Introduction to Test benches

(BT Level 6: Creating)

7.0 FPGA Implementation of Digital Design (9 Hours)

7.1 HDL Operators and Expressions
7.2 Data Flow-Level modelling
7.3 HDL Procedural Statements
7.4 Controlled Operation Statements
7.5 HDL Tasks and Functions
7.6 Targeting FPGA: Implement and Download

(BT Level 6: Creating)

References

1. Katz, "Contemporary Logic Design", 2nd Ed., USA: Prentice Hall.
2. Givone, "Digital Principles and Design", USA: McGraw-Hill.
3. Chu,P.P., "FPGA Prototyping by VHDL Examples: Xilinx Spartan-3 Version",, John Wiley & Sons, Inc

Assessment

Assignment	15%
Project	15%
Test	30%
Final Examination	40%
Total	**100%**

Assessment Methods

1: Assessment on Knowledge Domain (shorter duration)
- *Final Examination, Test, Quiz*

2: Assessment on Knowledge Domain (longer duration)
- *Assignment, Project*

3: Assessment on Skills and Affective Domains
- *Presentation, Laboratory Assessment, Demonstration, Self/Peer/Group Evaluation.*

4: Assessment on Report as Final Product
- *Thesis/Dissertation/Industrial Training Report*

Teaching Approach [Lecture and Discussion, Group Project, Active Learning, Cooperative Learning, Presentation]

Course Homepage http://notes.ump.edu.my/fkee/BEE3233/